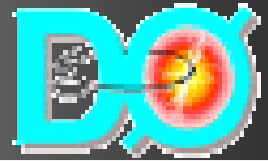


STT In-Crate CPU

Bill Lee

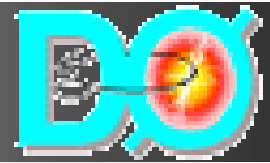
28 April 2000

CPU



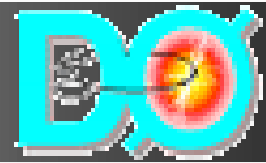
- **Motorola Power PC**
- **Running VxWorks 5.3d**
- **EPICS**
- **Does not communicate with TCC**

Tasks for the CPU



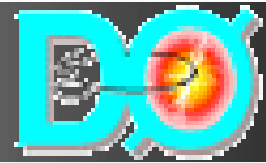
- **Downloading**
 - Initialization - Power on
 - Begin of Run Modifications
- **Monitoring**
 - CollectStatus
 - End of Run
- **Error Handling**

Initialization Tasks



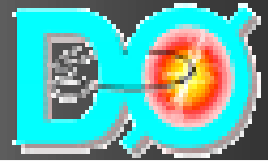
- **Initialize VME Memory Space**
- **Download Look-up Tables (LUT's) and Other Information**
 - **FRC - None?**
 - **STC - Gains, Pedestals, Road Conversion, thresholds (~0.5 MB? X 9)**
 - **TFC - Matrices (~1 MB X 2)**

Initialization Method



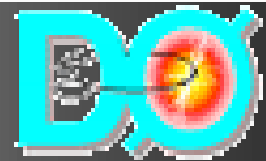
- **At power up and reboot**
 - CPU downloads its kernel
 - Runs start-up script
 - Initialize VME
 - Could download LUT's
 - Record of download???
 - Download DSP code

Initialization Method Cont.



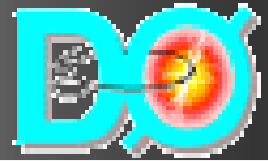
- **COOR can instruct the CPU through COMICS and EPICS to download**
- **Downloading of new FPGA code??**

Begin of Run Download



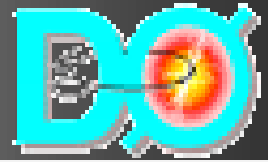
- **FRC - ??**
- **SMT**
 - **Bad Channel List**
 - **L3 and Monitor Readout Data-type**
- **TFC - ??**

Monitoring



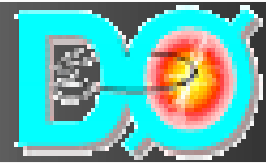
- Once every ~5s on *CollectStatus* FRC notifies CPU
- CPU reads data over VME/PCI busses
- Monitoring data should be stored in registers on the daughter cards
- CPU notifies FRC when finished with VME

Monitoring Data



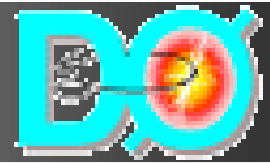
- **FRC - (256 Bytes)**
 - SCLF, RR, TRDF, BM
- **STC - ($\sim 10.5 \text{ kB} \times 9 = \sim 95 \text{ kB}$)**
 - Error counts, channel hits, # centroids, state occupancy, data sums
- **TFC - ($64 \text{ Bytes} \times 2 = 128 \text{ Bytes}$)**
 - I/O counts, DSP state, processing times, and processing data

Monitoring - Other Cards



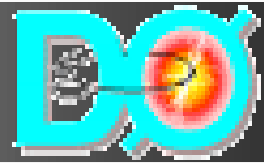
- **LRC - (~64 Bytes X 15?)**
 - word errors, FIFO occupancy
- **LTC ?**
- **VTM ?**
- **VBD ?**
- **Others**

Monitoring Path



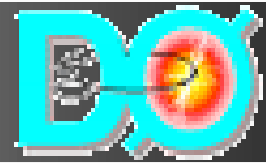
- **Uses Slow Controls**
- **Need to support additional monitoring requests to the CPU**

CPU Driven Monitoring



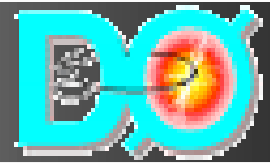
- **Additional monitoring information may be required at end of run**
 - requests would come from COOR to the CPU
- **User initiated monitoring**
- **User initiated clear**

Monitoring Problems



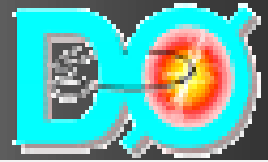
- **Inconsistent resetting of registers**
- **Possible VBD deadtime?**

Error Handling



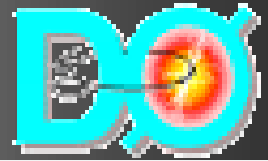
- **Hang Diagnostics**
- **Alarm conditions**
- **Link or card reset**
- **SCL INIT**

Tasks



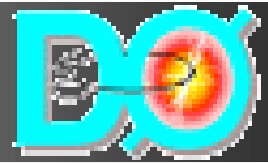
- **Create State machine for CPU**
- **Configure EPICS for STT**
- **Write COOR configuration files**
- **Design and write operator interface**
 - need to know Python
- **Write an STT monitoring class**

Tasks Cont.



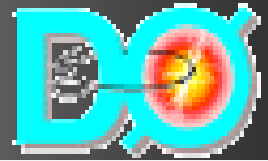
- **Pseudocode VxWorks modules**
- **Code**
- **Write various drivers**
 - **Setting up VME Bus**
 - **Talking to electronics**

Other Groups



- **We have been encouraged to consult with Silicon and L2 experts to borrow as much software as possible.**

Manpower



- **Me**
- **FSU Summer Student**
- **Possible new Dutch graduate student**